

What is claimed is:

1. A variable-gain digital filter having a construction in which a gain regulation circuit is incorporated inside the digital filter, said gain regulation circuit comprising: a first selector for
5 selecting gain; and a first multiplier for multiplying input data with a gain signal, which is output of said first selector.

2. A variable-gain digital filter according to claim 1 wherein:

said first multiplier of said gain regulation circuit multiplies a gain signal that is outputted from
5 said first selector with a coefficient sequence that is switched and outputted from a second selector for each fixed time interval;

the output of said first multiplier is multiplied at a second multiplier with input data that have
10 been selected by a third selector that selects and outputs from each output of a shift register; and

the output of said second multiplier is then integrated by an integrator and outputted.

3. A variable-gain digital filter comprising:
a shift register that is constituted by a plurality of stages of flip-flops and that both shifts

input data and generates delayed output by each stage;
5 a first selector for selecting gain;
 a second selector for selecting a coefficient
sequence;
 a third selector for selecting each delay output
of said shift register;
10 a first multiplier for multiplying output of
said first selector with output of said second selector;
 a second multiplier for multiplying output of
said first multiplier with output of said third selector;
and
15 an integrator for integrating output of said
second multiplier.

4. A variable-gain digital filter according to
claim 3 wherein:

 said first, second, and third selectors and said
first and second multipliers are doubled in quantity and
5 makes each of them handles divided half of the delayed
data; and

 each of said first to third selectors switch
output at each time interval of $(T/n) \times 2$, where T is the
duration of one time slot and n is the filter order.

5 A variable-gain digital filter according to
claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity and
5 divided loads half for each of said first to third selectors and said first and second multipliers ; and
each of said first to third selectors switch output at each time interval of T/n , where T is the duration of one time slot and n is the filter order.

6 A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are increase m times in
5 quantity to process each of them only n/m delayed data allowing the processing speed of multiplier for $1/m$.

7 A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are increase m times in
5 quantity to process each of them only n/m delayed data to improve the processing speed of the variable-gain digital filter.